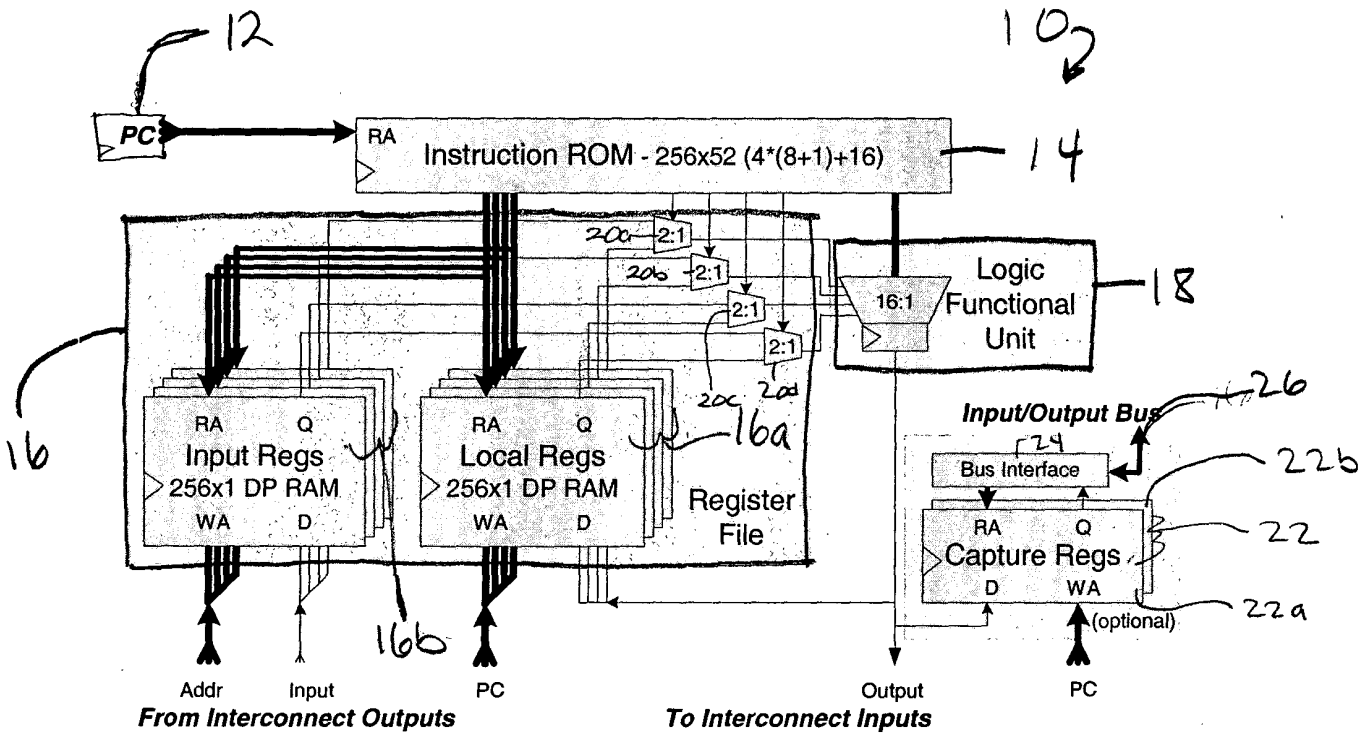
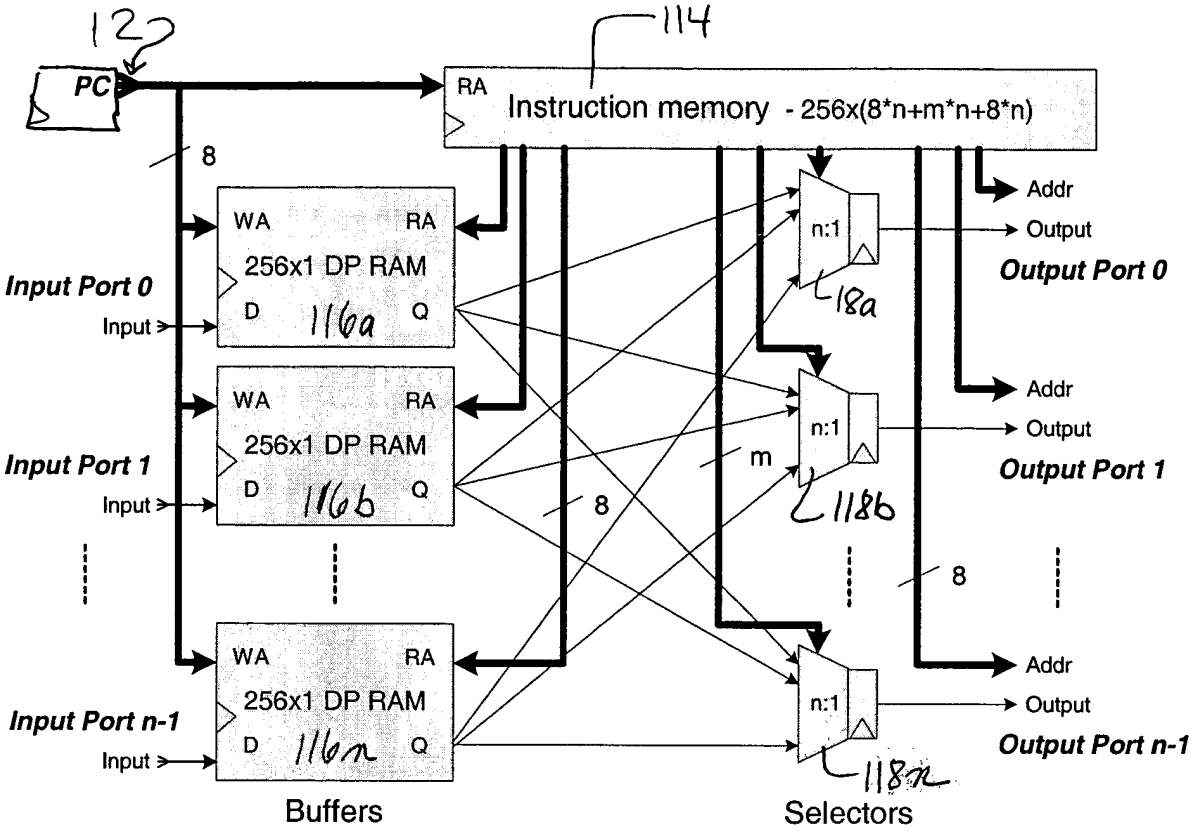


Fig. 1: Logic Processor for programming into FPGAs
(All memories and registers are synchronously clocked by the common system clock.)

Fig. 1


122
PC
114
RA
Instruction memory - 256x(8*n+m*n+8*n)
8
WA
RA
256x1 DP RAM
D
Q
116a
Input Port 0
Input
116b
Input Port 1
116n
Input Port n-1
Buffers
n:1
118a
118b
118n
m
8
Addr
Output
Output Port 0
Output Port 1
Output Port n-1
Selectors

100

Fig. 2

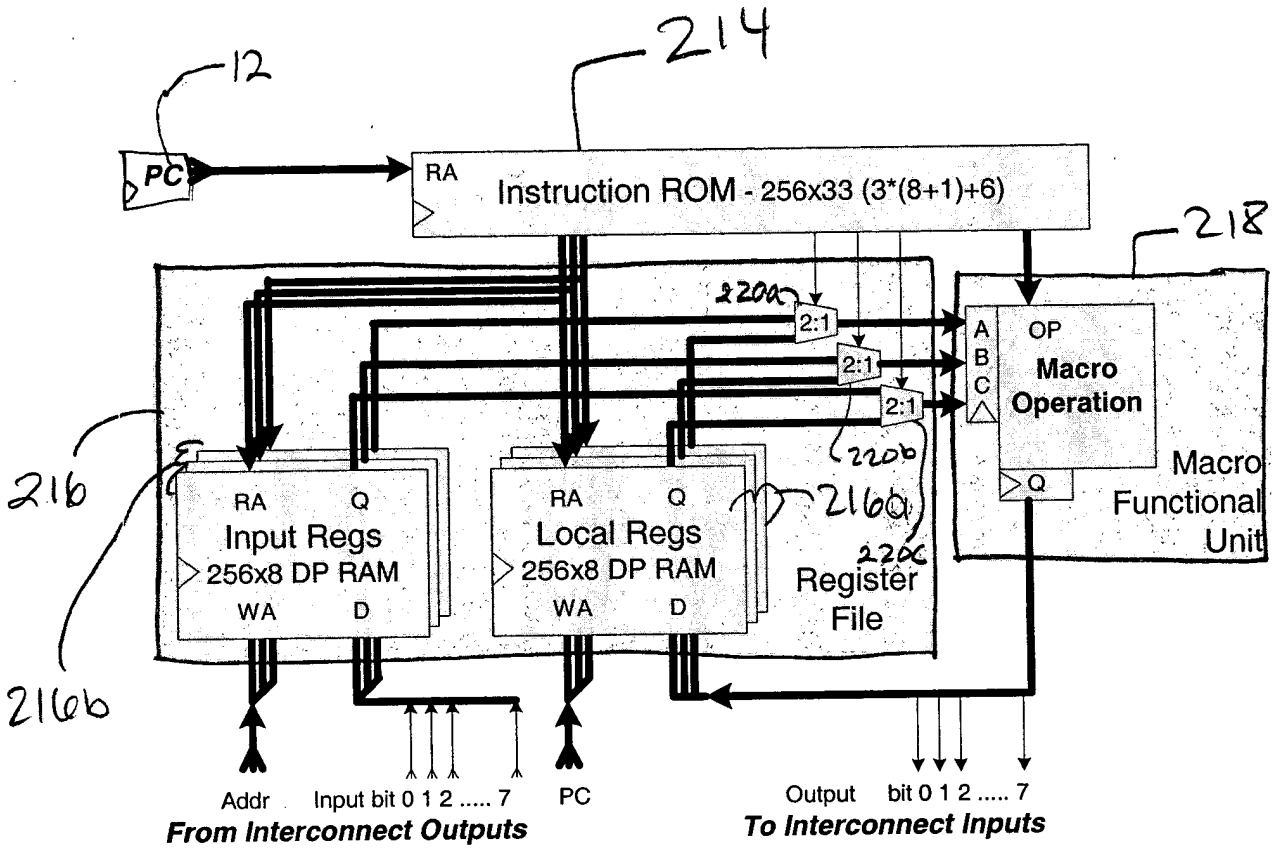


Fig. 3: Macro Processor

200

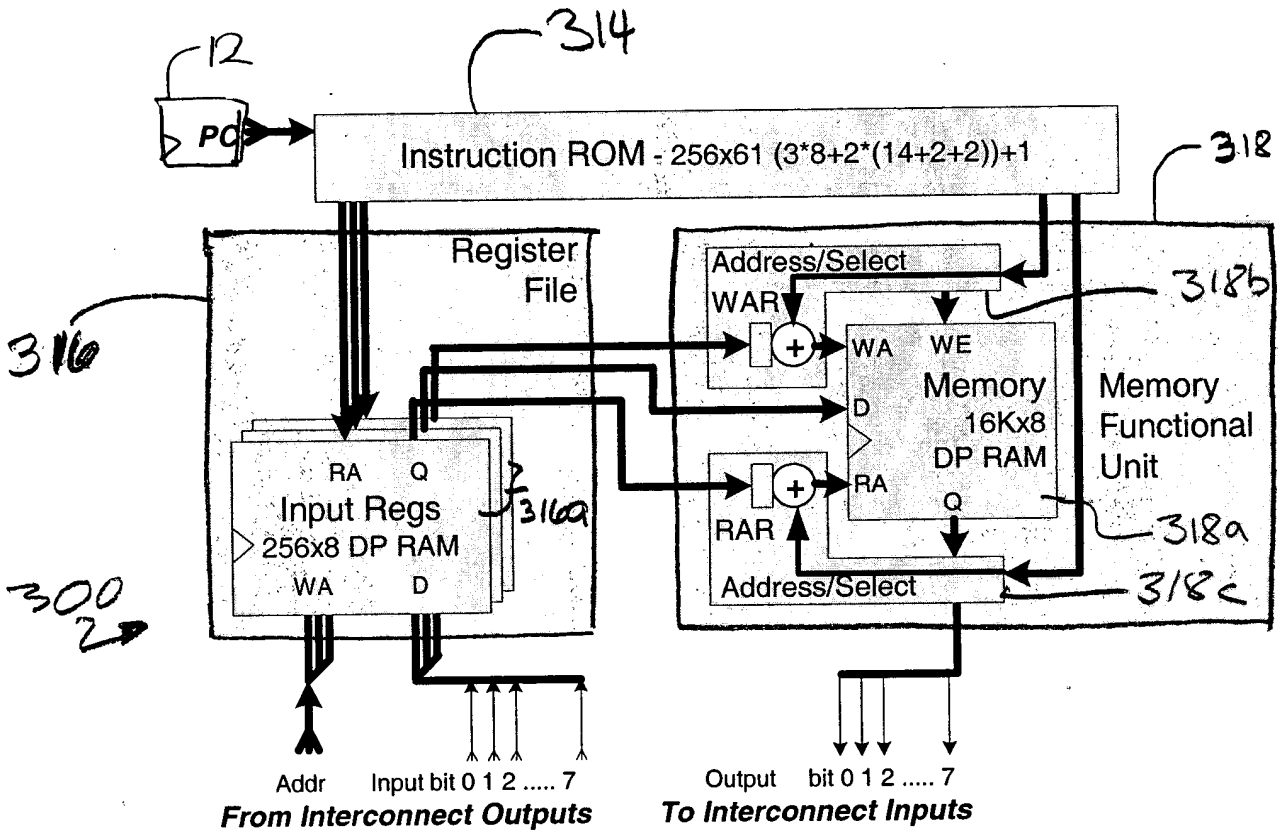


Fig. 4: Memory Processor

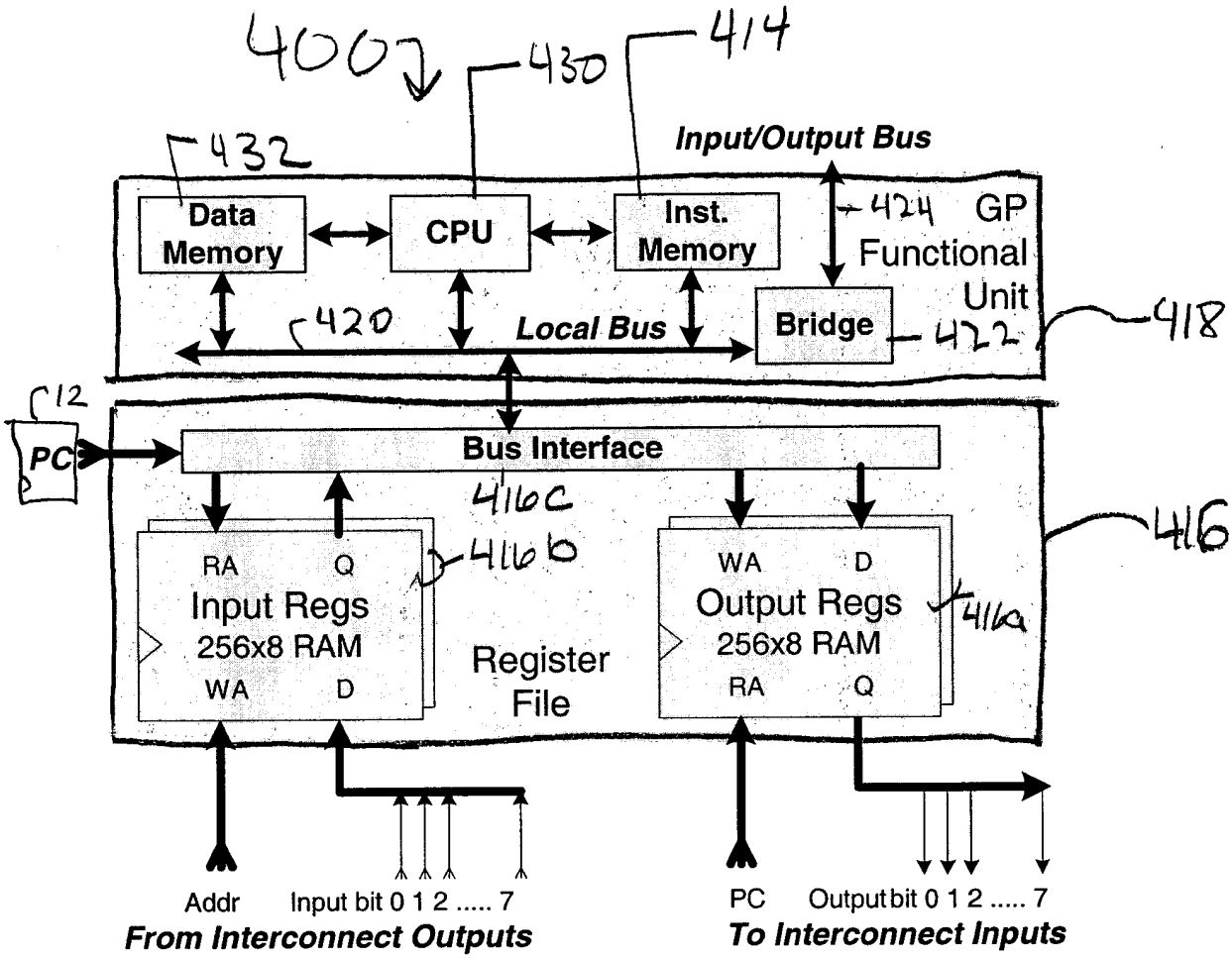


Fig. 5: General Purpose Processor

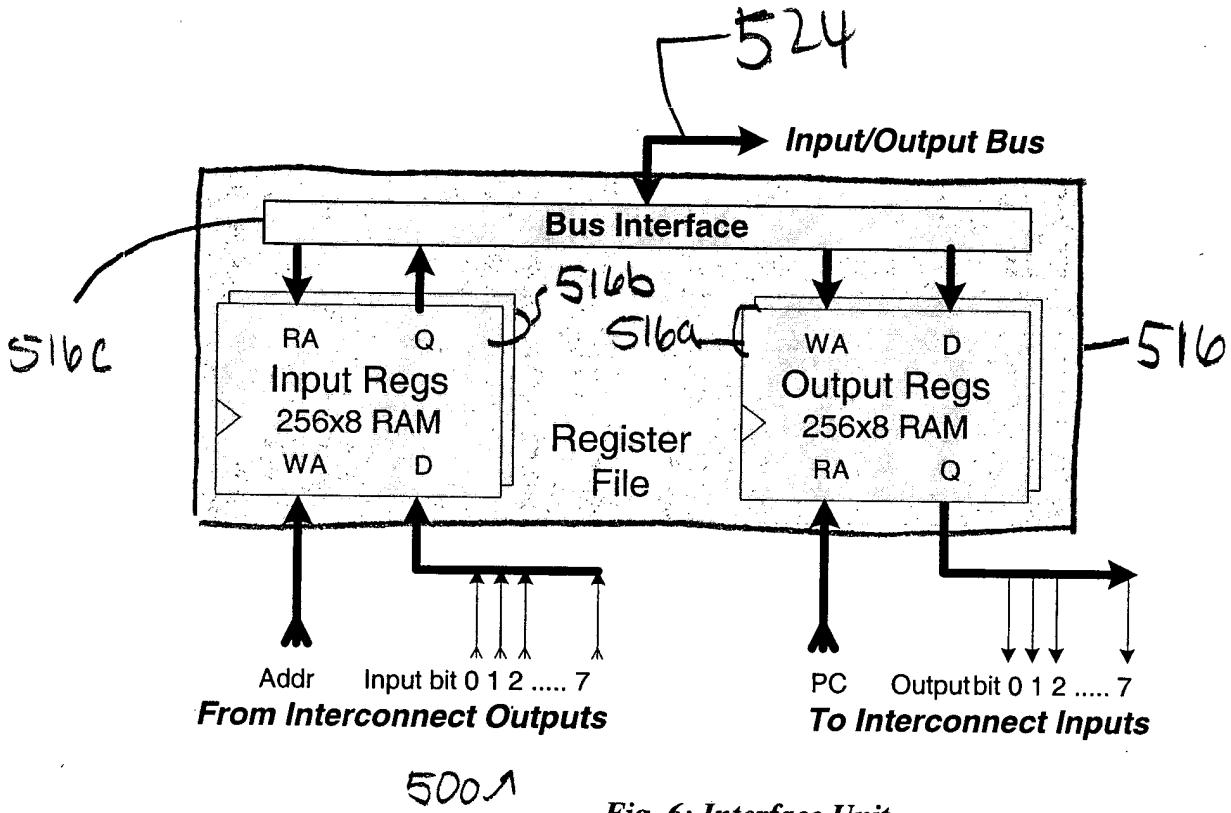


Fig. 6: Interface Unit

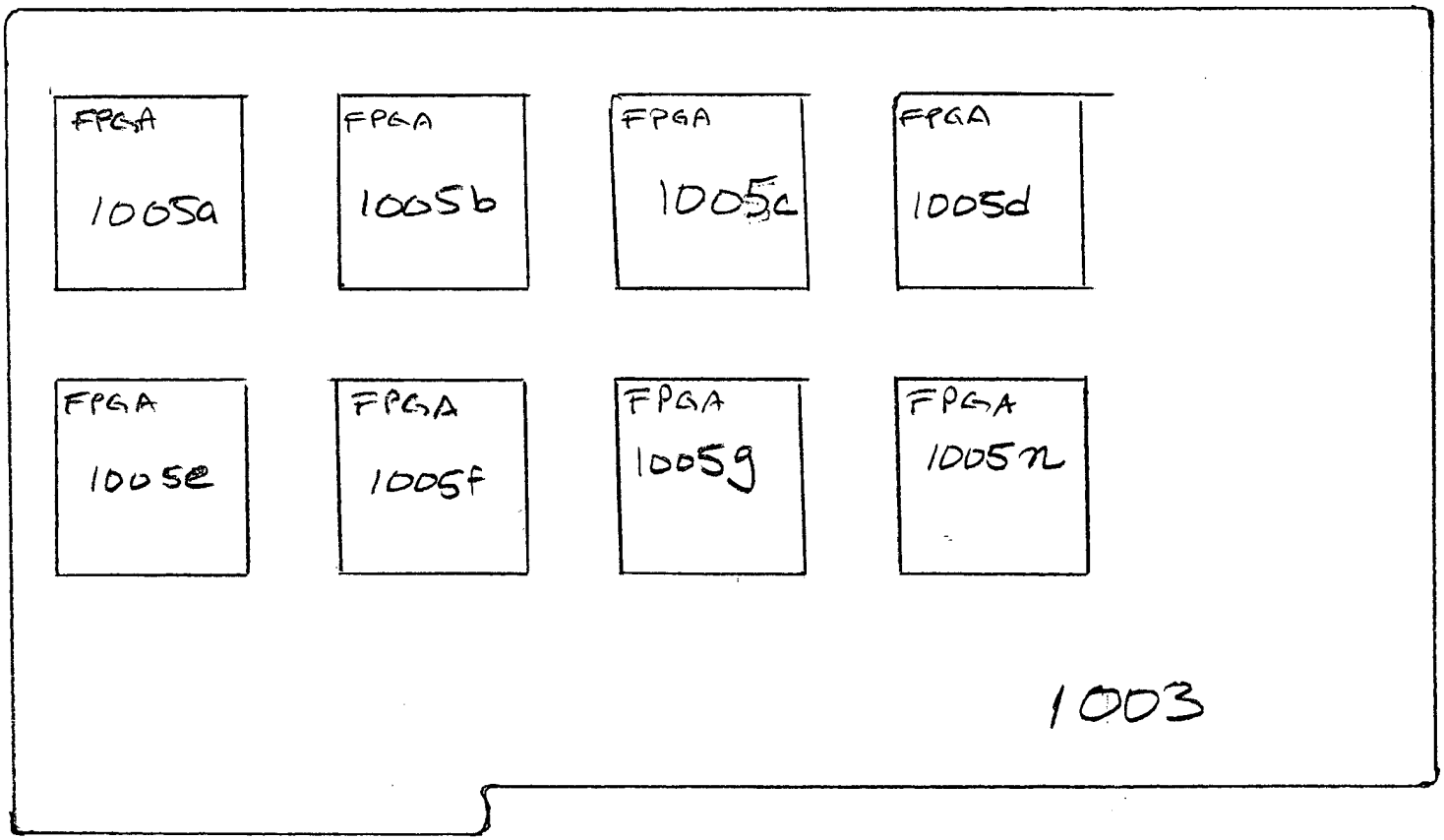


Fig. 7